

JAPANESE

[JP,2001-505367,A]

CLAIMS DETAILED DESCRIPTION DRAWINGS

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

1. Touch Process and the; Aforementioned Substrate Which are the Method of Producing Thin Film Electrode (79,329) Which Has Less Than 1 Micron in Sum Total Thickness, and Offer :Substrate (77,324). The process and the; aforementioned glue line which form the glue line (98,326) containing titanium are touched. The aforementioned method characterized by the process which anneals the aforementioned electrode which touches the aforementioned substrate for 5 minutes and 45 minutes at the temperature of 622 degrees C or more including the process and; which form the layer (81,328) of at least 8 times as thick noble metals as the thickness the aforementioned glue line.
2. The aforementioned annealing temperature is the method according to claim 1 of being a question (622 degrees C and 850 degrees C).
3. It is the method according to claim 2 which the aforementioned annealing temperature is 650 degrees C, and is further characterized by performing the aforementioned annealing for 30 minutes.
4. The process of the aforementioned annealing is a method according to claim 1 characterized by moving the aforementioned electrode which touches the aforementioned substrate all over an annealing furnace at lamp speed which reaches the aforementioned temperature within 10 minutes.
5. Touch Process and the; Aforementioned Substrate Which are the Method of Producing Thin Film Electrode (79,329) Which Has Less Than 1 Micron in Sum Total Thickness, and Offer :Substrate (77,324). The process and the; aforementioned glue line which form the glue line (98,326) containing a conductive material which has the minimum oxide eutectic temperature are touched. The process and; which form the layer (81,328) of different noble metals from the aforementioned glue-line material are included. It is characterized by the process which anneals the aforementioned electrode which touches the aforementioned substrate at the temperature more than the aforementioned minimum oxide eutectic temperature of the aforementioned glue-line material. the process of the aforementioned annealing The aforementioned method including moving the aforementioned electrode which touches the aforementioned substrate all over an annealing furnace at lamp speed which reaches the aforementioned temperature within 10 minutes.
6. The aforementioned lamp speed is a method according to claim 4 or 5 characterized by being what reaches the aforementioned temperature in 5 or less minutes.
7. It is the way according to claim 1 or 5 the aforementioned glue-line material is titanium, and the aforementioned noble metals are platinum.
8. The Second Different Material from Glue Line (98,326) Formed Using First Material and First Material of; above is Included. Electrode (79,329) for Using it in Integrated Circuit (100) — it is — : — It has the noble-metals layer (81,328) and; which have thickness T, and is characterized by the diffusion field (327) formed in the interface of the aforementioned glue line and the aforementioned noble-metals layer. this diffusion field The aforementioned diffusion field is the aforementioned electrode which it has thickness L and is $L \leq 0.5T$ including a field which the first material of the above diffuses in the aforementioned noble-metals layer.
9. Integrated-circuit electrode according to claim 8 characterized by $L \leq 0.25T$.
10. For the aforementioned noble metals, the aforementioned glue line is an integrated-circuit electrode containing platinum according to claim 8, including a titanium dioxide.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

The electrode structure and its production method of an integrated circuit Field of background 1. invention of invention this invention relates to such an electrode that uses noble metals for a detail combining a heat-resistant metal-bonding layer more about the electrode structure for the capacitor of an integrated circuit, and other thin film electronic elements.

2. Statement of technical problem The electrode formed using noble metals is widely used in an integrated circuit and other thin film electronic instruments. The noble-metals electrode is liked especially as an electrode of ferroelectric equipment like the ferroelectric capacitor used in a storage use, because the most effective ferroelectric is because it is the metallic oxides which need 850 degrees from the annealing temperature of about 600 degrees C in oxygen atmosphere. or [that such annealing generally oxidizes other metal: currently conventionally used for electrodes] — or the thing for which it fuses and the produced metallic oxides pollute CMOS structure — it is — moreover, a desirable thing — general — conductivity — a low When exposed to oxygen at an elevated temperature, since the noble metals like platinum have the capacity to hold the electrical conductivity which bore and was excellent in oxidization, it is ideal as an electrode. For example, the electrical conductivity of the platinum in the thin film whose thickness is 1000/ — 5000Å is about 0.5–0.8 ohms/square.

however — the latest integrated circuit and the latest thin film applicable field — a ferroelectric capacitor — a detached core (SiO₂), for example, a silicon dioxide, — a wrap — it is necessary to produce like Generally platinum and other noble metals are not well joined to such a detached core. For example, the degree of dissolution solution of the platinum in a silicon dioxide is zero. Therefore, it is because stress is caused by down stream processing which has the inclination which a mechanical failure like ablation produces, because an integrated circuit or other thin film electronic instruments follow when noble metals exist in contact with the front face of detached core. Although a glue line like titanium is generally deposited between a detached core and a noble-metals electrode in this reason, this is because there is capacity for a glue line to be spread in platinum and to react with a silicon dioxide. For example, please refer to U.S. Pat. No. 5,005,102 published by William.L.Larson on April 2, 1991.

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

The electrode structure and its production method of an integrated circuit Field of background 1. invention of invention this invention relates to such an electrode that uses noble metals for a detail combining a heat-resistant metal-bonding layer more about the electrode structure for the capacitor of an integrated circuit, and other thin film electronic elements.

2. Statement of technical problem The electrode formed using noble metals is widely used in an integrated circuit and other thin film electronic instruments. The noble-metals electrode is liked especially as an electrode of ferroelectric equipment like the ferroelectric capacitor used in a storage use, because the most effective ferroelectric is because it is the metallic oxides which need 850 degrees from the annealing temperature of about 600 degrees C in oxygen atmosphere. or [that such annealing generally oxidizes other metal: currently conventionally used for electrodes] — or the thing for which it fuses and the produced metallic oxides pollute CMOS structure — it is — moreover, a desirable thing — general — conductivity — a low When exposed to oxygen at an elevated temperature, since the noble metals like platinum have the capacity to hold the electrical conductivity which bore and was excellent in oxidation, it is ideal as an electrode. For example, the electrical conductivity of the platinum in the thin film whose thickness is 1000Å — 5000Å is about 0.5–0.8 ohms/square.

however — the latest integrated circuit and the latest thin film applicable field — a ferroelectric capacitor — a detached core (SiO₂), for example, a silicon dioxide, — a wrap — it is necessary to produce like Generally platinum and other noble metals are not well joined to such a detached core. For example, the degree of dissolution solution of the platinum in a silicon dioxide is zero. Therefore, it is because stress is caused by down stream processing which has the inclination which a mechanical failure like ablation produces, because an integrated circuit or other thin film electronic instruments follow when noble metals exist in contact with the front face of detached core. Although a glue line like titanium is generally deposited between a detached core and a noble-metals electrode in this reason, this is because there is capacity for a glue line to be spread in platinum and to react with a silicon dioxide. For example, please refer to U.S. Pat. No. 5,005,102 published by William.L.Larson on April 2, 1991. A glue line is diffused in noble metals, and reacts with a detached core by forming the oxide well joined to a detached core. However, the charge of a binder brings about the problem of the further stability, and the fall of electrical conductivity. For example, please refer to KSreenivas et al., Investigation of Pt/Ti bilayer metallization on silicon for ferroelectric thin film integration, J.of Applied Physics, Vol.75(1), and 1 January 1994 (it is not the conventional technology of this invention). it turns out that the glue line / noble-metals electrode of the combination of all in the conventional technology produce most number of a hillock (hillock), a void, and other defects (this gathers the resistivity of an electrode and reduces reliability) Furthermore, titanium is diffused very promptly in platinum, in the midst of the annealing processing which continues in many cases, passes through platinum completely and forms ***** on the surface of platinum. K. Please refer to the Sreenivas et al. above and p.235. Therefore, the structure and the method of bringing about the good electrical conductivity and good stability of an electrode for the ferroelectric and other materials which need oxygen annealing in an elevated temperature are required.

Summary of invention this invention offers the outstanding noble-metals electrode by solving the above-mentioned technical problem and making the amount of the charge of a binder in a glue line into the minimum. this invention makes the minimum the rutile oxides in the charge of a binder again.

According to this invention, you should make the layer of the charge of a binder below into 500Å (Å) in thickness. Preferably, the thickness of a glue line is for 25Å and 500Å.

The ratio of the thickness pair noble-metals layer thickness of a glue line is 1:10 or less. An electrode is preferably annealed at lamp speed which anneals at high lamp speed in oxygen, namely, reaches an annealing temperature by 5 or less minutes most preferably in less than 10 minutes.

It anneals at lamp speed to which it continues, and has the layer of about 2000Å platinum, and this electrode reaches [the layer of the titanium of about 200Å thickness with which the optimal electrode was formed in contact with the silicon-dioxide detached core for the silicon-dioxide detached core, and] an annealing temperature in about 5 or less minutes in about 650 degrees C and oxygen.

this invention offers the method of producing the thin film electrode which has less than 1 micron in sum total thickness, and this method touches the process and the; aforementioned substrate which offer :substrate. Touch the process and the; aforementioned glue line which form the glue line containing a conductive material, and it differs from the aforementioned glue-line material. The process and; which anneal the aforementioned electrode which touches the process which forms the layer of at least 8 times as thick noble metals as the thickness of the aforementioned glue line, and the; aforementioned substrate at the temperature more than the minimum oxide eutectic temperature (minimum oxide eutectic temperature) of the aforementioned glue-line material are included. Preferably, the process which forms a glue line includes that thickness forms the layer between 25Å and 500Å.

The aforementioned noble-metals layer is preferably at least 10 times as thick as the aforementioned glue line. The process of the aforementioned annealing includes preferably moving the aforementioned electrode which touches the aforementioned substrate all over an annealing furnace at lamp speed which reaches the aforementioned temperature within 10 minutes. The aforementioned lamp speed seems to reach the aforementioned temperature in 5 or less minutes preferably. As for the aforementioned glue line, the aforementioned noble metals contain platinum including titanium preferably. The aforementioned titanium layer thickness is 200Å or less preferably, and the aforementioned platinum layer thickness is at least 2000Å. Preferably, the aforementioned annealing temperature is for 622 degrees C and 850 degrees C, and performs the aforementioned annealing between 5 minutes and 45 minutes. Most preferably,

the aforementioned annealing temperature is 650 degrees C, and performs the aforementioned annealing for 30 minutes. In another mode, this invention offers the method of producing the thin film electrode which has less than 1 micron in sum total thickness, and this method touches the process and the; aforementioned substrate which offer :substrate. The aforementioned electrode which touches the process and the; aforementioned glue line which form the glue line containing a conductive material, and touches the process which forms the layer of different noble metals from the aforementioned glue-line material, and the; aforementioned substrate. The process of the aforementioned annealing includes moving the aforementioned electrode which touches the aforementioned substrate all over an annealing furnace at lamp speed which reaches the aforementioned temperature within 10 minutes including the process and; which anneal at the temperature more than the minimum oxide eutectic temperature of the aforementioned glue-line material. The aforementioned lamp speed seems to reach the aforementioned temperature in 5 or less minutes preferably. The aforementioned glue-line material is titanium preferably, and the aforementioned noble metals are platinum. The aforementioned annealing temperature is for 622 degrees C and 850 degrees C preferably. The aforementioned annealing is preferably performed with the question for 5 minutes and 45 minutes. Preferably, the aforementioned annealing temperature is 650 degrees C, and performs the aforementioned annealing for 30 minutes.

this invention offers the ferroelectric capacitor of an integrated circuit equipped with the ferroelectric material between the first electrode, the second electrode, and the aforementioned first and the second electrode again, and the first electrode of the above is formed in contact with the glue line and the; aforementioned glue line containing the layer of the material to 500A in thickness, and is equipped with at least 8 times as thick the noble-metals layer and; containing a different material from the aforementioned glue-line material as the aforementioned glue line. The aforementioned noble-metals layer is preferably at least 10 times as thick as the aforementioned glue line. As for the aforementioned glue line, the aforementioned noble metals contain platinum including a titanium dioxide preferably. The aforementioned titanium oxide layer thickness is to 200A preferably, and the aforementioned platinum layer thickness is at least 2000A.

In still more nearly another mode this invention The first electrode and the second electrode, The ferroelectric capacitor of an integrated circuit equipped with the ferroelectric material between the aforementioned first and the second electrode is offered. The first electrode of the above is between the glue line and the; aforementioned ferroelectric material which were formed using the :first material, and the aforementioned glue line. It has the diffusion field and; which were formed in the interface of the noble-metals layer and the; aforementioned glue line which have thickness T, and the aforementioned noble-metals layer including the second different material from the first material of the above. this diffusion field The aforementioned diffusion field has thickness L including a field which the first material of the above diffuses in the aforementioned noble-metals layer, and it is; $L \leq 0.5T$. It is $L \leq .25T$ preferably. As for the aforementioned glue line, the aforementioned noble metals contain platinum including a titanium dioxide preferably.

In the further mode, this invention offers the electrode for using it combining ferroelectric material in an integrated circuit. This electrode is between the glue line and the; aforementioned ferroelectric material which were formed using the :first material, and the aforementioned glue line. It has the diffusion field and; which were formed in the interface of the noble-metals layer and the; aforementioned glue line which have thickness T, and the aforementioned noble-metals layer including the second different material from the first material of the above. this diffusion field The aforementioned diffusion field has thickness L including a field which the first material of the above diffuses in the aforementioned noble-metals layer, and it is; $L \leq 0.5T$. It is $L \leq .25T$ preferably. As for the aforementioned glue line, the aforementioned noble metals contain platinum including a titanium dioxide preferably.

Furthermore, in another mode, this invention offers the electrode for using it combining ferroelectric material in an integrated circuit, this electrode is between the glue line and the; aforementioned ferroelectric material containing the layer of material with a thickness of less than 500A, and the aforementioned glue line, and it has the noble-metals layer and; containing a different material from the aforementioned glue-line material. The aforementioned noble-metals layer is preferably at least 8 times as thick as the aforementioned glue line. As for the aforementioned glue line, the aforementioned noble metals contain platinum including a titanium dioxide preferably.

Moreover, in the further mode, this invention offers the electrode for using it combining ferroelectric material in an integrated circuit, this electrode is between :glue line, the; aforementioned ferroelectric material, and the aforementioned glue line, and it has at least 8 times as thick a noble-metals layer and; as the aforementioned glue line including a different material from the aforementioned glue-line material. As for the aforementioned glue line, the aforementioned noble metals contain platinum including a titanium dioxide preferably. this invention offers the electrode for using it combining ferroelectric material in an integrated circuit further, this electrode is equipped with the layer containing titanium, and this layer is to 400A in thickness. The aforementioned layer is to 200A in thickness preferably. It turns out over several years that the above-mentioned electrode is effective by stability. If a lamp rise is quickly carried out to the temperature which exceeds the minimum oxide eutectic formation temperature of a titanium dioxide, i.e., 622 degrees C, according to research of this electrode, diffusion of the titanium to many portions of platinum will be restricted near titanium / the platinum interface by what (tie up) titanium is quickly fixed for in a titanium dioxide. The amount of TiO_2 which exists that titanium is little is restricted, and rapid annealing prevents formation of the rutile phase $2O_4$ of titanium oxide, i.e., Ti, and Ti_3O_6 grade. TiO_2 has the cubical-expansion ratio 9:5 as compared with titanium, and a rutile phase has a still higher coefficient of cubical expansion. Therefore, with restricting the amount of a titanium dioxide, especially a rutile phase, stress is reduced more and a hillock, a void, and the number of other defects are reduced greatly.

Easy explanation of a drawing Drawing 1 is the flow chart showing the main processes of the method of forming the electrode by this invention.

Drawing 2 is the cross section of the suitable example of a DRAM integrated-circuit memory cell made using the electrode structure and the production method of this invention.

Drawing 3 is the plan of a silicon wafer, and the thin film capacitor by this invention on this front face of a wafer is expanded very much, and is shown.

Drawing 4 is a part of cross section of drawing 3 cut with the line 4-4 which shows the thin film capacitor equipment by this invention.

Drawing 5 shows the detail of the drawing 2 and the lower electrode structure of the capacitor of 3 and 4 which show the mode of an electrode important for this invention.

Detailed explanation of a suitable example Drawing 2 shows a part of typical integrated circuit 100 using the electrode by this invention. This part shown is 1T/1C containing a transistor 72 and a capacitor 80. The DRAM/FERAM memory cell 76 is included. A memory cell 76 is a FERAM memory cell, when it is a DRAM memory cell when a layer 82 is a dielectric, and a layer 82 is a ferroelectric. Therefore,

this invention persons make this the DRAM/FERAM cell 76 containing a dielectric / ferroelectric layer 82, or only call it a memory cell 76. A capacitor 80 is formed in contact with the thick insulating layer 77 which separates a capacitor from a transistor 72. It is required to prevent separating the ferroelectric / dielectric 82 of a capacitor from a transistor 72, and the atom in a ferroelectric/dielectric moving to the silicon of a transistor, or when desirable, especially this example is desirable for a ferroelectric or dielectric materials, for example, ABO₃ type oxides, and stratified superlattice material (layered superlattice materials). the substrate 71 to which an integrated circuit 100 is located downward — a single crystal silicon wafer (a transistor 72 is formed in the front face) is included preferably. A transistor 72 is equipped with the source / drain active regions 73A and 73B which were formed by doping to many fields of the substrate 71 located downward, and the gate 74. An integrated circuit 100 contains further the field area of exposed oxide 75 and the first insulating layer 77 by which a capacitor 80 is formed on a front face. Although these are formed in a process which is mutually different as everyone knows including a gate oxide and a thermal oxidation object, since it is made from the same material, the first insulating layer 77 is essentially unified. The first insulating layer 77 may contain other layers further explained to U.S. Pat. No. 5,468,684 published on November 21, 1995. A capacitor 80 contains the first electrode 79, the ferroelectric/dielectric layer 82, and the second electrode 84. The first electrode 79 contains a glue line 98 and noble metals 81. The wiring layer 88 which exists on a capacitor 80 and is often called metallization layer connects active-region 73B to the first electrode 81 of a capacitor 80, and the second insulating layer 86 connects active-region 73A and the second electrode 84 to other portions of a circuit. A wiring layer 88 is multilayer structure preferably. this structure in the field 90 which contacts active regions 73A and 73B preferably in the case of annealing processing although preferably made from platinum each front face 99 and 97 of the second layer 91 currently made from titanium as preferably as the layer 89 which forms silicification platinum, and the electrodes 81 and 84 of a capacitor is contacted — it is preferably made from platinum — 93 [layer / third] is included. The capping layer 95 is a desirable hermetic material like silicon nitride or acid silicon nitride, or are a non-doped silicon dioxide and another layer of SOG which carried out the phosphorus dope, and makes the layer structure of an integrated circuit perfect. Again, for the reason, especially this invention examines the structure and the production method of such an electrode in a detail more below about the method of producing an electrode 79. Other portions may be produced so that it may be indicated by U.S. Pat. No. 5,468,684 published on November 21, 1995, or you may produce them by other arbitrary conventional methods. As everyone knows, generally an integrated circuit, 100 [for example,], is produced on a wafer front face, a wafer is succeedingly cut to the individual integrated circuit chip of hundreds, and each chip contains the cell 76 of thousands or millions. Next, the packaging of each chip is carried out and the completed integrated circuit is obtained.

In the following examination, this invention persons examine the method of this invention according to the example of DRAM/FERAM in drawing 2. This is because it is the suitable example of the electronic instrument 100 using the structure and the method of this invention. However, it is understood that this invention predicts that it can be used even if it combines this method with the example of other DRAM/FERAM and many of other electronic instruments using a thin film electrode. Furthermore, it is understood that the actual capacitor which the capacitor of drawing 2 is formed by that it is useful generalization in order to show the rough relation between [some / other] a capacitor and its part, and an integrated circuit, and the method of this invention, and uses the structure of this invention may have a different gestalt a little.

In the industry of an integrated circuit, being used often vaguely understands the term a "substrate." Often, this is used in order to point out 71 of the silicon with which an integrated circuit is produced by the front face, gallium arsenide, or other wafers, for example drawing 2. This invention persons called this above "substrate located downward." In other cases, this term is used and the incomplete portion of the integrated circuit by which a specific layer is formed in a front face is pointed out to them. For example, in this meaning, the "substrate" by which the capacitor 80 of drawing 2 is formed in a front face is an incomplete integrated circuit to a layer 77 from a general standpoint. In further others, the word of a "substrate" is used, and the layer in which the material in a front face is formed and which adjoined is meant in it. In this meaning, a layer 77 is a substrate by which a capacitor 80 is formed in a front face and which adjoined. In this specification, the term "substrate" is used widely and the arbitrary layers by which other layers are formed in a front face are meant. When a capacitor like 80 of drawing 2 was being examined especially, it adjoined most. "substrate" is a layer 77, and is a layer 77 and many layers under it more widely. When a barrier layer like the ferroelectric / dielectric layer 82 of drawing 2 is being examined, the "substrate" which adjoined most is the noble-metals layer 81, and is the larger lower electrode 79 and all the larger layers of the incomplete integrated circuit under it.

Seeing from the standpoint of an integrated circuit and meaning a thin film understands the term the "thin film" in this indication. That is, the term a "thin film" is sometimes used in the equipment (macroscopic) industry of macroscopic level as what means a film with a thickness of less than about 100 microns. Generally, so-called such "thin film" is thickness in which the thinnest thing also exceeds 1 micron. Such a film is always thinly made with an integrated circuit from the standpoint of an integrated circuit by the method not suiting. In this indication, a "thin film" means the film which is less than 1 micron in thickness, and is less than 0.5 microns in thickness preferably.

When it changes to drawing 1, a flow chart shows many processes of the desirable method by this invention. The typical wafer 300 (drawing 3 -5) which has already produced the qualification-test sample of the thin film capacitor equipment of an integrated circuit according to this invention examines this method. It understands such drawing that it is idealized drawing used in order that it may not become a plan or a cross section with a certain specific actual portion of an actual capacitor and a possible twist may also clearly and fully describe the structure and the method of this invention by the option. It is the cross section of the wafer 300 of drawing 3 cut with the line 4-4 which is shown in drawing 4. ** [reference of drawing 1, and 3, 4 and 5 / contain / the P type silicon substrate 322 offered in the process 10 (drawing 1) / preferably / a wafer 300] In a process 12, steam growth of about 5000Å silicon-dioxide insulating layer 324 is carried out. Next, in a process 14, it is the spot preferably on silicon-dioxide 324 front face about the thin glue line 326 (inch situ).

It deposits by sputtering. By titanium, a layer 326 is 500Å or less in thickness, and is a layer of titanium with a thickness of 200Å most preferably. Next, in a process 16, the noble-metals layer 328 (drawing 5) of thickness T is deposited. Although noble metals are platinum preferably, palladium or other arbitrary noble metals are sufficient. A layer 328 is preferably at least 10 times as thick as a glue line 326. Most preferably, this is 2000Å platinum 328 and is deposited by sputtering on that spot. I hear that both titanium and platinum carry out spatter membrane formation, without breaking a vacuum, and that the "spot" means has it. Since titanium reacts with a silicon dioxide, and it is spread in platinum, and it oxidizes here and the titanium of the minimal dose is used so that it may inquire in detail to the following, a titanium dioxide is essentially continuous into platinum from the inside of silicon, and it helps for platinum 328 to paste this up on a silicon dioxide 324. An electrode 329 is annealed in a process 18. This annealing is preferably performed in plus

pushing and drawer time for 45 minutes from 5 minutes between 450 degrees C and 850 degrees C all over an oxygen furnace. Preferably, a wafer is introduced in a furnace above 5 inches per minute in lamp speed, and this serves as temperature lamp speed which rises from the initial temperature of about 100 degrees C - 150 degrees C, and reaches a perfect annealing temperature in less than 10 minutes from the standpoint of temperature. Most preferably, at 100%, oxygen is the flow of 5l. per minute, lamp speed is 9.0 inch per minute, and it is the time for, as for this, the temperature lamp speed from initial temperature (100 degrees C - 150 degrees C) to the temperature of 650 degrees C of a furnace becoming 5 or less minutes, and sum total annealing time pushing in plus EREFANT (elephant) in a furnace for 30 minutes, and pulling out. Instead, you may use oxygen by reduced pressure of less than 1 atmospheric pressure. In annealing processing, distance L diffusion of titanium is done into platinum. Titanium is diffused in a silicon dioxide, reacts with a silicon dioxide again, and forms mixed film 326' (drawing 5) of a titanium dioxide and a silicon dioxide. Near the interface with the thick silicon-dioxide layer 324, layer 326' is mainly a silicon dioxide, and some silicon formed by being mainly a titanium dioxide and returning a silicon dioxide to others near the interface with a layer 327, including some silicon formed by returning a silicon dioxide to others is included. Within the limits of the diffusion length L, titanium turns into a titanium dioxide which exists along with the grain boundary of platinum crystal grain. Distance L — 1/ of thickness T of the platinum layer 328 — it is between 0.1 of the thickness of platinum, and 0.25 times preferably two or less. Next, an integrated circuit is completed in a process 20. This completion process includes forming the layer 330 of a ferroelectric or dielectric materials by processing explained to the following in detail, and forming the second electrode 332. The second electrode 332 is the layer of 2000A platinum 332, and is preferably formed by sputtering. However, this is good as a multilayer electrode, for example, the layer of platinum, the layer of another metals, such as a tungsten or nickel, and layer of aluminum. Or it is good as other electrode structures of some kind. Material 330 is stratified superlattice material, for example a tantalum-acid strontium bismuth, a niobic-acid strontium bismuth tantalum, and a niobic-acid barium bismuth preferably. The perfect explanation about stratified superlattice material is shown in U.S. Pat. No. 5,519,234 published by this invention persons on May 21, 1996. Material 330 is good again as an ABO₃ type perovskite, for example, BST and PZT, or other metallic-oxide material. A wafer 300 is again annealed after deposition of material 330, pattern formation is carried out using the photo-mask method, it ***** to the electrode layer 328, and the capacitor equipments 317A, 317B, and 317C of the rectangle of various sizes separated by the electrode 328 of latus area etc. are made (drawing 3). The size of Equipments 317A, 317B, and 317C etc. is exaggerated very much by drawing 3 . The examination of each equipments 317A, 317B, and 317C etc. can be performed by making the narrow probe which connected or lead of a testing device to the platinum-electrode layer 328, and connected other electrode layers 332, such as the specific equipments 317A, 317B, and 317C, to other leads of a testing device contact.

Production of the typical equipment of the type shown in drawing 3 -5 is explained in detail in the following example. Before each explanation, the table which lists the reactant component used by the production method is, each is followed and there is explanation of a ferroelectricity and/or a dielectric property suitably.

The solvent to be used is explained within explanation of processing after each **. In a table, "FW" shows formula weight, "g" shows gram, "mmole" shows the millimole and "Equiv." shows the number of the equivalents of the mol in a solution. "Xylenes" shows the xylene solution of three different judgment of a xylene, i.e., marketing which only contains Para, meta (meda), or an ortho xylene in instead of. bismuth 2-ethylhexanoate — the bismuth solution of the commercial bismuth 2-ethylhexanoate in 74% naphtha — being shown —; — formula weight is shown in a parenthesis in this case, this is the equivalent formula weight of the bismuth in the solution as the whole, and only taking into consideration existence of not the formula weight of bismuth 2-ethylhexanoate but naphtha is shown. All processings were performed with the atmospheric pressure of Colorado Springs and Colorado, unless it refused especially. All the initial wafer substrates from which the material explained was produced by the front face in the six examples of the following start. It is a stratified substrate and this is shown by layers 322, 324, 326, and 328 by drawing 4 . after the electrode annealing process 18. It is seen to layers 322 and 324, 326', and 327 and 328 as [show / in drawing 5]. moreover, the silicon substrate 322. It had the field oxide-film layer 324 which produced and carried out wet growth with the P type silicon of the resistivity between 5 ohm-cm and 25 ohm-cm and which was made into about 5000A, the layer 326' with a thickness [of the titanium which carried out spatter membrane formation] of 200A, and the 2000A layer 328 of the platinum which carried out spatter membrane formation. After depositing so that layers 330 and 332 may be explained in an example, the positive type or the negative-mold photoresist was used combining the photo-mask process, and as shown in drawing 3 , pattern formation of the wafer 300 was carried out. When an example is indicated to be a positive-type photoresist, the spin coat of the resist is carried out by 5000RPM, and a postbake is continuously carried out the prebake of the 95 degrees C for 2 minutes and performed at 140 degrees C for 7 seconds by the standard photo-mask method on a hot plate for UV exposure, 1-minute development, 1-minute rinsing, and 5 minutes. When an example is indicated to be a negative-mold photoresist, the spin coat of the negative resist is carried out by 5000RPM, and a postbake is continuously carried out the prebake of the 90 degrees C for 5 minutes and performed at 140 degrees C for 4 seconds by the standard photo-mask method on a hot plate for UV exposure, 1-minute development, 1-minute rinsing, and 5 minutes. When it is indicated as IPC ablation, this is oxygen plasma ablation, and it is Ion. Plasma Corporation "a barrel etcher" is used by 500m torr oxygen and 350W. When it is indicated as rapid heat treatment (rapid thermal process) (RTP), it is AG about processing. Associates model 410Heat Carrying out using Pulser, the given lamp speed uses temperature for the time zone which raises even a working temperature, and the given time is a time zone which holds temperature to a working temperature. In all cases, a part for oxygen flow 3 l./is used in RTP annealing.

Example 1 Tantalum-acid strontium bismuth-SrBi₂Ta₂O₉ It measured about the compound shown in Table I.

化合物	FW	g	mmole	Equiv.
タンタルエトキシド	406.26	4.9553	12.197	2.0000
2-エチルヘキサン酸	144.21	8.7995	61.019	10.006
ストロンチウム	87.62	0.5330	6.0831	0.9975
2-エチルヘキサン酸	144.21	1.7613	12.213	2.0026
ビスマス2-エチル ヘキサノエート	(862.99)	10.525	12.196	1.9998

表 I

Strontium was set by the first measurand of 2-ethyl hexanoic acid, and the 80ml 2-methoxyethanol. Mixture was agitated by the low fever between about 70 degrees C and 90 degrees C, and the reaction rate was enlarged. After making all strontium react, when a solution was mostly cooled to a room temperature, tantalum ethoxide was added, and the second measurand of 2-ethyl hexanoic acid was added continuously. Mixture was agitated, and it heated at 115 degrees C of maximum temperatures, and distillation removal of ethanol and the water was carried out. Next, 75ml xylenes were added, and bismuth 2-ethylhexanoate was added continuously. The solution was agitated, and it heated at about 125 degrees C of maximum temperatures, and left only the 60.0ml solution. Concentration is per [0] liter.

It was 102-mol SrBi₂Ta₂O₉. The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer 300 which deposited the layer to the platinum lower electrode 328 like drawing 4 , the eyedropper (eyedropper) was used and 2OSrBi₂Ta₉ 1ml solution was placed. The spin of the wafer was carried out for 20 seconds 1500 RPM. Next, BEKU [the wafer was placed on the hot plate and] for 3 minutes in about 250 degrees C and air. Even the process [BEKU / on a hot plate / process / process / which make a solution deposit on a wafer using an eyedropper] / was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed by 750 degrees C and oxygen flow 5 l/m for 2 hours. the up layer 332 of 2000A platinum — spatter membrane formation — carrying out — a resist — applying — continuing — the standard photo-mask method and an ion mill — dirty (ion mill etch), IPC ablation, and the last contact annealing were performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m It turns out that the obtained sample is examined and it has the polarizability which can disregard defatigation over 1010 cycle. In comparison with the material of the conventional technology, such a result is a surprising thing and shows that this capacitor is considered to continue indefinitely in ferroelectric switching memory.

By the newer sample, the precursor solution in the xylenes using concentration SrBi[of 0.2 mols]₂Ta₂O₉ which was explained above was diluted to 0.13 mols using n-butyl acetate, next, carried out the spin coat on the wafer, and as explained above, it was processed. When it examined, the value of two 2Pr was cm² the 23.39 and 25.06 whole microcoulombs among samples, respectively defatigation has not only been disregarded by such sample, but, and this was uncommonly high as compared with the conventional technology. Example 2 Niobic-acid strontium bismuth-SrBi₂Nb₂O₉ It measured about the compound shown in Table II.

化合物	FW	g	mmole	Equiv.
ストロンチウム	87.62	0.5625	6.4198	1.0000
2-エチルヘキサン酸	144.21	2.0940	14.520	2.2618
ビスマス2-エチル ヘキサノエート	(862.99)	11.079	12.838	1.9998
ニオブブトキシド	458.48	5.8862	12.839	1.9999
2-エチルヘキサン酸	144.21	9.2911	64.428	10.036

表Ⅱ

Strontium was placed into the 30ml 2-methoxyethanol. The first measurand of 2-ethyl hexanoic acid was added, and it was made to react completely. Bismuth 2-ethylhexanoate was added, and 35ml xylenes were added continuously. Niobium butoxide and the second measurand of 2-ethyl hexanoic acid were added, and 40ml xylenes were added continuously. Mixture was heated and agitated and all butanols, water, and the 2-methoxyethanol were removed at about 123 degrees C of maximum temperatures. The last volume was 63n and the last mass was 57.475g. Concentration was 0.1117m mol SrBi2Nb 2O9 per gram of 0.102 mols [per liter] SrBi2Nb 2O9, i.e., a solution.

The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer which deposited the layer to the platinum, lower electrode 328 like drawing 4, the eyedropper was used and 2OSrBi2Nb9 1ml solution was placed. The spin of the wafer was carried out for 20 seconds 1000 RPM. Next, BEKU [the wafer was placed on the hot plate and] for 2 minutes and 30 seconds in 230 degrees C and air. Even the process [BEKU / on a hot plate / process / process / which deposits 2OSrBi2Nb9 solution on a wafer using an eyedropper] / was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed for 40 minutes by 750 degrees C and oxygen flow 5 l/m. Spatter membrane formation of the up layer 332 of 2000A platinum was carried out, the negative resist was applied, and the standard photo-mask method, ion mill dirty, IPC ablation, and the last contact annealing were continuously performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m. The obtained sample was examined. This sample was the ferroelectric which was [for account *****] excellent, and was a "high-speed" switching material comparatively.

Example 3 Niobic-acid strontium bismuth tantalum-SrBi2Ta NbO9 It measured about the compound shown in Table III.

化合物	FW	g	mmole	Equiv.
ストロンチウム	87.62	0.5821	6.6435	1.0001
2-エチルヘキサン酸	144.21	1.9770	13.709	2.0635
ビスマス2-エチル ヘキサノエート	(862.99)	11.4687	13.289	2.0005
タンタルブトキシド	546.522	3.6303	6.6426	1.0000
ニオブブトキシド	458.48	3.0456	6.6428	1.0000
2-エチルヘキサン酸	144.21	9.6081	66.626	10.030

表Ⅲ

After placing strontium into a 30ml 2-methoxyethanol, the first measurand of 2-ethyl hexanoic acid was added, and it was made to react completely. Next, bismuth 2-ethylhexanoate was added, and 40ml xylenes were added continuously. Tantalum butoxide and niobium butoxide were added, and the second portion of 2-ethyl hexanoic acid and the xylenes of a 40ml addition were added continuously. Mixture was agitated, and it heated at 122 degrees C of maximum temperatures, distillation removal of all water, a butanol, and the 2-methoxyethanol was carried out, and it left the 65ml solution. Concentration was 0.102 mols [per liter] SrBi₂TaNbO₉. The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer which deposited the layer to the platinum lower electrode 328 like drawing 4, the eyedropper was used and SrBi₂TaNbO₉ 1ml solution was placed. The spin of the wafer was carried out for 20 seconds 1000 RPM. Next, BEKU [the wafer was placed on the hot plate and] for 5 minutes in 250 degrees C and air. The wafer was placed into the rapid thermal treatment equipment, and it annealed for 30 seconds at oxygen flow 3 l/m, the temperature of 700 degrees C, and 125 degrees [/second] lamp speed.

From a process to RTP which places SrBi₂TaNbO₉ solution on a wafer using an eyedropper was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed by 750 degrees C and oxygen flow 5 l/m for 2 hours. Spatter membrane formation of the up layer 332 of 2000A platinum was carried out, the positive resist was applied, and the standard photo-mask method, ion mill dirty, IPC ablation, and the last contact annealing were continuously performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m. The obtained sample was examined and defatigation was again hardly shown. A new examination does not show defatigation in essence up to 1012 cycle, but, as for this, about 1 million times are better than the material of the best conventional technology rather than it can set in the sample (it produced using the bismuth with 10% - 20 superfluous%) of a tantalic-acid strontium bismuth and a niobic-acid strontium bismuth tantalum.

Example 4 Tantalic-acid barium bismuth-BaBi₂Ta₂O₉ It measured about the compound shown in Table IV.

化合物	FW	g	mmole	Equiv.
バリウム	137.327	0.9323	6.7889	1.0000
2-エチルヘキサン酸	144.21	1.9733	13.684	2.0156
ビスマス2-エチル ヘキサノエート	(862.99)	11.717	13.577	1.9999
タンタルブトキシド	546.522	7.4211	13.579	2.0002
2-エチルヘキサン酸	144.21	9.9216	68.800	10.314

表IV

After placing barium into a 40ml 2-methoxyethanol and 20ml toluene and making a reaction late, the first measurand of 2-ethyl hexanoic acid was added, and it was made to react completely. Next, bismuth 2-ethylhexanoate was added, and 40ml xylenes were added continuously. The solution was agitated, and it heated at about 123 degrees C of maximum temperatures, and distillation removal of water, toluene, and the 2-methoxyethanol was carried out. The solution was cooled to the room temperature, next tantalum butoxide was added, and the second portion of 2-ethyl hexanoic acid and the xylenes of a 40ml addition were added continuously. Heating and agitating mixture in temperature of about 123 degrees C, distillation removal of the butanol was carried out and it left the 66ml solution. Concentration was 0.103 mols [per liter] BaBi₂Ta₂O₉. The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer which deposited the layer to the platinum lower electrode 328 like drawing 4, the eyedropper was used and 2OBaBi₂Ta₉ 1ml solution was placed.

The spin of the wafer was carried out for 20 seconds 1000 RPM. Next, BEKU [the wafer was placed on the hot plate and] for 5 minutes in 250 degrees C and air. The wafer was placed into the rapid thermal treatment equipment, and it annealed for 30 seconds at oxygen flow 3 l/m, the temperature of 700 degrees C, and 125 degrees [/second] lamp speed. From a process to RTP which places 2OBaBi₂Ta₉ solution on a spinner using an eyedropper was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed by 750 degrees C and oxygen flow 5 l/m for 2 hours. Spatter membrane formation of the up layer 332 of 2000Å platinum was carried out, the positive resist was applied, and the standard photo-mask method, ion mill dirty, IPC ablation, and the last contact annealing were continuously performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m. The obtained sample was examined and the result shown in drawing 8 was obtained.

BaBi₂Ta₂O₉ was not a switching ferroelectric but paraelectrics, and was specific inductive capacity 166 in 1MHz. This is very high specific inductive capacity as compared with the specific inductive capacity 3.9 of the silicon dioxide which is the dielectric most generally used in an integrated circuit. The leakage current curve of 2OBaBi₂Ta₉ sample is also excellent, and it has ignored by the low battery, i.e., the order of 10⁻¹⁰ A/cm². The leakage current which covers the range of the voltage used in the conventional integrated circuit, namely, crosses a 2400A sample by 1-10 volts stops less than [about 10 - 8A //cm] at two, and this is still very much more small.

Example 5 Tantalum-acid lead bismuth-PbBi₂Ta₂O₉ It measured about the compound shown in Table V.

化合物	FW	g	mmole	Equiv.
キシレン類中の 鉛 2-エチル ヘキサノエート	(1263.6)	16.691	13.209	1.1000
ビスマス 2-エチル ヘキサノエート	(753.35)	18.095	24.019	2.0002
タンタルブトキシド	546.52	13.126	24.017	2.0001
2-エチルヘキサン酸	144.21	17.967	124.59	10.375

表V

The lead 2-ethylhexanoate in the xylenes which are the stock solution produced beforehand, and bismuth 2-ethylhexanoate were doubled, and 40ml xylenes were doubled continuously. Next, tantalum butoxide was added, and 2-ethyl hexanoic acid was added continuously. Mixture was agitated for 4 hours by the low fever between about 70 degrees C and 90 degrees C, next, was raised to 110 degrees C of maximum temperatures, distillation removal of the butanol was carried out, and it left the 66ml solution. Concentration was 0.172 mols [per liter] PbBi₂Ta 2O₉, and 10% of lead was superfluous. The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer which deposited the layer to the platinum lower electrode 328 like drawing 4, the eyedropper was used and 2OPbBi₂Ta₉ 1ml solution was placed. The spin of the wafer was carried out for 20 seconds 1000 RPM. Next, half [2 minutes and] BEKU [the wafer was placed on the hot plate and] in 375 degrees C and air. Even the process [BEKU / process / which places 2OPbBi₂Ta₉ solution on a wafer using an eyedropper / process] was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed for 90 minutes by 750 degrees C and oxygen flow 5 l/m. Spatter membrane formation of the up layer 332 of 2000A platinum was carried out, the negative resist was applied, and the standard photo-mask method, ion mill dirty, IPC ablation, and the last contact annealing were continuously performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m. Although the sample was examined, it was specific inductive capacity 114 in 1MHz and this was smaller than the thing of BaBi₂Ta 2O₉, in addition than the dielectric for the conventional semiconductors, they were 30 to 40 times. Although the leakage current was more large, it was the value is less than [10 - 7A //cm] two, and it was still excellent / value / in this within the limits of general voltage in the integrated circuit in addition in the case of the electric field of less than about 500 kv/cm. Since big resistance is acquired to radiation damage when lead exists, this material is especially interesting. Many elements which blend and make this material are also conformable in comparison with the conventional integrated-circuit material.

Example 6 Niobic-acid barium bismuth-BaBi₂Nb 2O₉ It measured about the compound shown in Table VI.

化合物	FW	g	mmole	Equiv.
バリウム	137.327	0.9419	6.8588	1.0000
2-エチルヘキサン酸	144.21	2.0538		
ピスマス 2-エチル ヘキサノエート	(862.99)	11.838	13.717	1.9999
ニオブブトキシド	458.48	6.2894	13.718	2.0001
2-エチルヘキサン酸	144.21	10.051	69.697	10.162

表VI

It was made to react completely, adding and agitating the first measurand of 2-ethyl hexanoic acid, after placing barium into a 30ml 2-methoxyethanol and 20ml toluene and making a reaction late. Next, bismuth 2-ethylhexanoate was added, and 50ml xylenes were added continuously. Mixture was agitated, and it heated at about 118 degrees C of maximum temperatures, and distillation removal of all water, toluene, and the 2-methoxyethanol was carried out. The solution was cooled to the room temperature, next niobium butoxide was added, and the second portion of 2-ethyl hexanoic acid and the xylenes of a 30ml addition were added continuously. Heating and agitating mixture in temperature of 124 degrees C, distillation removal of all the butanols and water was carried out, and it left the 68% solution. Concentration was 0.101 mols [per liter] BaBi2Nb 2O9. The wafer, and it dehydrated. [in 140 degrees C and air] [for 30 minutes] On the wafer which deposited the layer to the platinum lower electrode 328 like drawing 4, the eyedropper was used and 2OBaBi2Nb9 1ml solution was placed. The spin of the wafer was carried out for 20 seconds 1000 RPM.

Next, BEKU [the wafer was placed on the hot plate and] for 2 minutes in 230 degrees C and air. The wafer was placed into the rapid thermal treatment equipment, and it annealed for 30 seconds at oxygen flow 3 l/m, the temperature of 700 degrees C, and 125 degrees [/second] lamp speed. From a process to RTP which places 2OBaBi2Nb9 solution on a wafer using an eyedropper was repeated about another layer. Next, the wafer was moved to the diffusion furnace and it annealed by 750 degrees C and oxygen flow 5 l/m for 1 hour. Sputter membrane formation of the up layer 332 of 2000A platinum was carried out, the negative resist was applied, and the standard photo-mask method, ion mill dirty, IPC ablation, and the last contact annealing were continuously performed for 30 minutes by 750 degrees C and oxygen flow 5 l/m. The obtained sample was examined and it was specific inductive capacity 103.46 in 1MHz. Although this is lower than the specific inductive capacity of BaBi2Ta 2O9 and PbBi2Ta 2O9, it is still very much more high. Again, in addition, in the case of the electric field of less than about 300 kV/cm, the result of the leakage current was still every less than two 10 - 6A cm, although not excelled BaBi2Ta 2O9 and about 2O9 PbBi2Ta.

In the remaining example, stratified superlattice material was deposited using the Myst deposition method (misted deposition process) so that it might be explained to U.S. Pat. No. 5,456,945 published on October 10, 1995. The titanium layer 326 (drawing 4) was not used by some of such samples. In the case of the example which used the titanium glue line, the yield of a capacitor which passed was always far high. As shown above, in all the examples that used titanium, the titanium layer was about 200A in thickness, and the platinum layer 328 was about 2000A in thickness.

Example 7 It measured about the compound shown in Table VII.

化合物	FW	g	mmole	Equiv.
タンタルブトキシド	546.52	52.477	96.020	2.0000
2-エチルヘキサン酸	144.21	87.226	604.85	12.598
ストロンチウム	87.63	4.2108	48.052	1.0009
ビスマス 2-エチル ヘキサノエート	(790.10)	87.702	104.67	2.1802

表VII

Tantalum butoxide and 2-ethyl hexanoic acid were placed into the flask, and the xylenes of about 50ml (ml) were added. Mixture was agitated for 48 hours by the low fever between about 70 degrees C and 90 degrees C. After adding strontium, the solution was again agitated by the low fever and was made to react completely. Distillation removal of the butanol was carried out raising and agitating temperature at a maximum of 120 degrees C next, and it left about 40ml distilland. Next, after adding bismuth 2-ethylhexanoate, it diluted to 240ml using xylenes. Concentration was 0.200 mols [per liter] $\text{SrBi}_2\text{Ta}_2\text{O}_9$. This precursor was stored until use preparatio was completed.

The 4ml tantalic-acid strontium bismuth precursor explained above just before deposition was placed into the gray goods from Myst with the 10ml methyl-ethyl-ketone (MEK) initiator. The substrate 325 containing the silicon wafer 322 which the layer 324 of a silicon dioxide and the layer 328 of platinum have deposited on a front face was placed on the substrate electrode holder in a deposition chamber. In this case, there was no titanium layer 326. BEKU [$\text{SrBi}_2\text{Ta}_2\text{O}_9$ was deposited by the Myst deposition method, next, the wafer 300 was taken out from the deposition chamber, and it placed on the hot plate, dried for 2 minutes at the temperature of 150 degrees C, and / the temperature of 400 degrees C] for 5 minutes next. Next, the wafer 300 was moved to rapid heat treatment over and RTP was performed for 30 seconds at 750 degrees C here. Next, the wafer 300 was returned to the deposition chamber, Myst wa: formed again, UV was irradiated at Myst and the wafer 300, and the deposition process was repeated. RTP processing of the second layer was performed in 725 degrees C and 30 seconds and in oxygen. Next, the wafer 300 was annealed in oxygen for 1 hour. The obtained film 330 was about 2100A in thickness (A).

two or more capacitors 317A and 317B electrically connected by the lower electrode 328 were produced by what IC equipment 300 is completed, namely, spatter membrane formation of the second platinum electrode 332 is carried out, and is *****ed in a wafer next after the second annealing using well-known photoresist technology

About the tantalic-acid strontium bismuth capacitor produced by the above-mentioned method, the circuit of a non-compensated SOYA-tower was used by 10,000 Hertz by the voltage of 1 volt, 1.5 volts, 2 volts, 2.5 volts, 3 volts, and 5 volts, and hysteresis measurement was performed. A hysteresis curve is longwise, and it is an enclosed type, and it was shown that a capacitor is considered to operate perfect within storage. They were 20.9 microcoulombs / cm^2 in polarizability, 2Pr, **, and 5-volt measurement. They were maintenance voltage (coercive voltage), 2Vc, **, and 1.66 volts. The leakage current measured about the same sample is square cm the whole about 7×10^{-8} A in 5 volts, and it is the result of excelling which shows that it is thought that operation which it was still more sharply lower than operation on low voltage, and this excelled in this material within storage again is carried out more. Another sample was produced like the above-mentioned example 7, except that a substrate 325 contained the layer 326 of 200A thickness of titanium. The polarizability in 5 volts was 12.9 microcoulombs / cm^2 . Maintenance voltage and 2Vc were measured and it was 2.16 volts. The measured leakage current was 5×10^{-8} in 5 volts.

It turns out by the case of platinum / titanium electrode that the yield is far good. In the case of the lower electrode of only platinum, the abbreviation moiety of equipment connected too hastily, and one was not short-circuited when it was platinum / titanium lower electrode on the other hand.

Except having carried out [in the case of the platinum lower electrode sample] preliminary annealing of the substrate 325 in oxygen for 650 degrees C and 30 minutes for 800 degrees C and 30 minutes in the case of the inside of oxygen, and the Ti/Pt sample, as shown in the example of the above-mentioned Myst deposition, the further example of a tantalic-acid strontium bismuth capacitor was produced. Although the yield fell to about 10% only in the case of the lower electrode sample of only platinum, 2Pr value went up to 21.6 microcoulombs / cm^2 . Although the yield was still in state of 100% in the case of the Ti/Pt lower electrode, polarizability fell in 11.8 microcoulombs / cm^2 .

Example 8 Tantalum butoxide was replaced with niobium isopropoxide, the niobic-acid strontium bismuth precursor was produced, although it was the same method as the tantalic-acid strontium bismuth precursor of an example 7, and except having added to the tantalic-acid strontium bismuth precursor, as explained to the example 7, the sample of the niobic-acid strontium bismuth tantalum capacitor equipped with the Ti/Pt lower electrode was produced. The niobic-acid strontium bismuth precursor of a certain amount was added, and **** 50/50 of tantalum pair niobium was given in the precursor. The thickness of the obtained ferroelectric layer 330 was

crossed to the range of 1900 to 2300A, polarizability was crossed to the range of 11.7 microcoulombs / cm² to 12.5 microcoulombs / cm² by 5 volts, and 136 kilovolts [cm] / and 5x10 - 6A / of 1x10 - 5A / of leakage currents were [cm / cm] 2 from 2 in 5 volts from maintenance electric field, 2Ec, and 124 volts [/cm] **.

Example 9 It measured about the compound shown in Table VIII.

化合物	FW	g	mmole	Equiv.
タンタルブトキシド	546.52	52.4650	96.020	2.0000
2-エチルヘキサン酸	144.21	87.222	604.83	12.600
ニオブイソプロポキシド	388.35	11.184	28.799	0.6000
ストロンチウム	87.63	5.0490	57.617	1.2003
2-エチルヘキサン酸	144.21	24.710	171.35	3.5698
ビスマス2-エチル ヘキサノエート	(753.08)	105.44	140.01	2.7802

表Ⅷ

Tantalum butoxide and niobium isopropoxide were placed into the flask with the first measurand of 2-ethyl hexanoic acid, and the xylenes of about 50ml (ml). Mixture was agitated for 48 hours by the low fever between about 70 degrees C and 90 degrees C. The second measurand of 2-ethyl hexanoic acid was added, and strontium was added continuously. The solution was again agitated by the low fever and was made to react completely. Distillation removal of the butanol was carried out raising and agitating temperature at a maximum of 120 degrees C next, and it left about 40ml distilland. Next, after adding bismuth 2-ethylhexanoate, it diluted to 260ml using xylenes. Concentration was 0.200 mols [per liter] Sr1.2Bi2.78TaNb 0.4O9. This precursor was stored until use preparation was completed.

The 4ml niobic-acid strontium bismuth tantalum precursor explained above just before deposition was placed into the container 54 of the Myst generating machine 46 with the 10ml methyl-ethyl-ketone (MEK) initiator.

This precursor was used, and as the sample of the capacitor equipped with titanium / platinum lower electrode was explained to the example 7, it produced. By one sample, 12.7 microcoulombs / cm², maintenance electric field, 2Ec, 166 kilovolts [/cm] **, and 5x10 - 5A / of leakage currents of the thickness of a film 330 were [cm] 2 in 5 volts at 2150A, polarizability, 2Pr, and 5 volt of **. By another sample, 14.7 microcoulombs / cm², maintenance electric field, 2Ec, 166 kilovolts [/cm] **, and 4x10 - 7A / of leakage currents of the thickness of a film 330 were [cm] 2 in 5 volts at 2050A, polarizability, 2Pr, and 5 volt of **.

Example 10 The sample of further some was produced like an example 9 except having been n-butyl acetate instead of the last solvent added just before placing a precursor into the gray goods from Myst being a methyl ethyl ketone. Although the equipment of better quality was obtained by adding butyl acetate with xylenes as a common solvent in some cases, the reaction is not fully understood yet. Generally, n-butyl acetate soaks a substrate in fitness from xylenes, and is considered to bring about a better step coverage. By both samples, the thickness of a film 330 is 1850A. one side By polarizability, 2Pr, and 5 volt of **, 14.1 microcoulombs / cm², maintenance electric field, 2Ec(s), 182 kilovolts [/cm] **, and 1x10 - 7A / of leakage currents are [cm] 2 in 5 volts. another side 12.9 microcoulombs / cm², maintenance electric field, 2Ec, 199 kilovolts [/cm] **, and 3x10 - 7A / of leakage currents were [cm] 2 in 5 volts at polarizability, 2Pr, and 5 volt of **.

The electrode produced as explained in the above-mentioned sample continued having stability and high conductivity over many years through the examination of 1013 cycle at a room temperature and the elevated temperature of no less than 150 degrees C. According to subsequent analysis, it is shown that layer 326' which remains after annealing does not contain non-oxidized titanium as a matter of fact. Therefore, there is no titanium which is considered to move up through platinum 328 and to change the electronic property of a capacitor since all titanium is fixed in an oxide and "which separated" as a matter of fact. Furthermore, it turns out that the great portion of titanium oxide is a titanium dioxide. Therefore, the big expansion coefficient of rutile phase oxides is avoidable. As the above-mentioned example was shown, you should make thickness of the noble-metals layer 328 into 10 times of the thickness of the titanium layer 326 preferably. When relative thickness is under 10 to 1 (platinum pair titanium), some titanium has strong possibility of not oxidizing. This may reduce the yield and/or electrical property of equipment greatly. Furthermore, a hillock is formed

when the distance "L" in drawing 5 exceeds 0.5 times of thickness T of the platinum layer 328. Moreover, the resistivity of an electrode increases as the diffusion length L increases. Therefore, it is very important that the thickness of titanium 326 is farther [than the thickness of platinum 328] small. Furthermore, the minimum thickness of platinum 328 must be more than the double precision of the diffusion length greatly and preferably from the diffusion length of titanium.

It is absolutely small, namely, important that it is [of a glue line 326 being not only thin to the noble-metals layer 328 but a glue line also for 25A and 500A. Otherwise, since the amount of the titanium oxide in the field of the platinum grain boundary becomes very large, according to the difference of the expansion coefficient between titanium oxide and platinum 328, a hillock and other defects generate and an electrode becomes unstable.

Moreover, at the electrode annealing process 18, it is important for temperature higher than the minimum oxide eutectic temperature the charge of a binder to carry out a lamp rise quickly, namely, it is the lamp speed which reaches a perfect annealing temperature within 10 minutes, and equipment should be inserted into the furnace. Otherwise, even when the charge 326 of a binder is a film, before material oxidizes, it may be completely diffused through noble metals 328, and the rutile phase of an oxide may generate it by oxidation. Both results are made into the instability of an electrode and an electronic property is reduced.

The electrode by this invention is very stable, and it had the electrical conductivity of 1.0 ohms/square from 0.7 ohms/square, and when the antagonism of this was carried out to the electrical conductivity of the electrode of only platinum, things understood it. Although what is considered the suitable example of this invention and now has been explained, that it can carry out in other specific forms can understand this invention, without deviating from the pneuma or main features. For example, other charges of a binder, for example, a ruthenium, may be used instead of titanium, and the charge of a binder may form a different compound from oxides depending on a substrate. Therefore, in all modes, don't pass over this example to mere instantiation, and don't interpret it in limitation. An attached claim does not show the range of this invention, and it is not restrained at all by above-mentioned explanation.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

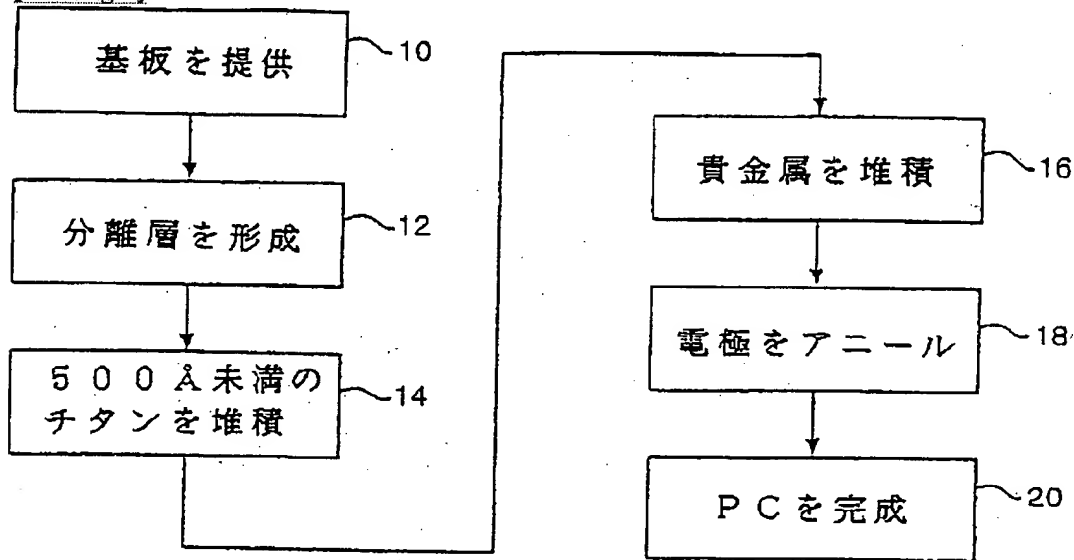


FIG. 1

[Drawing 2]

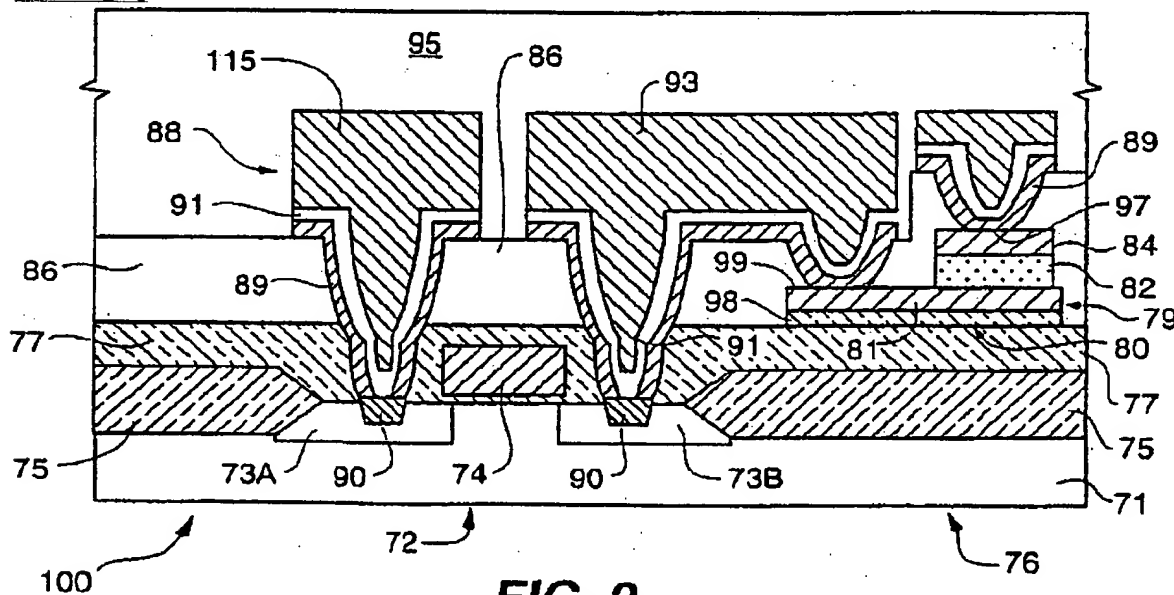
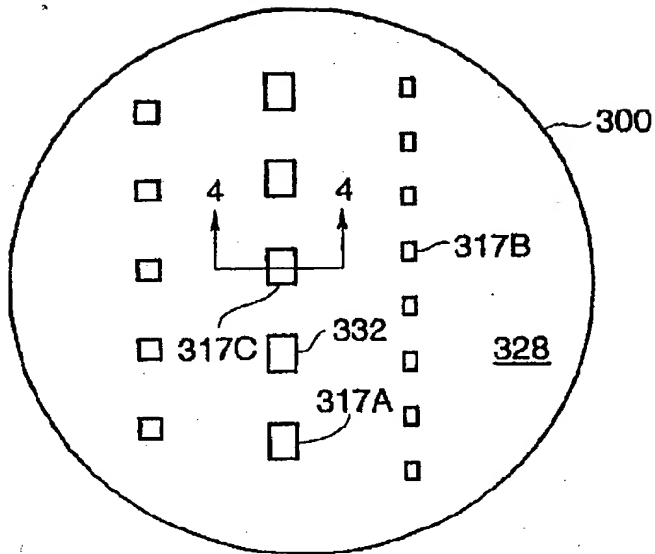
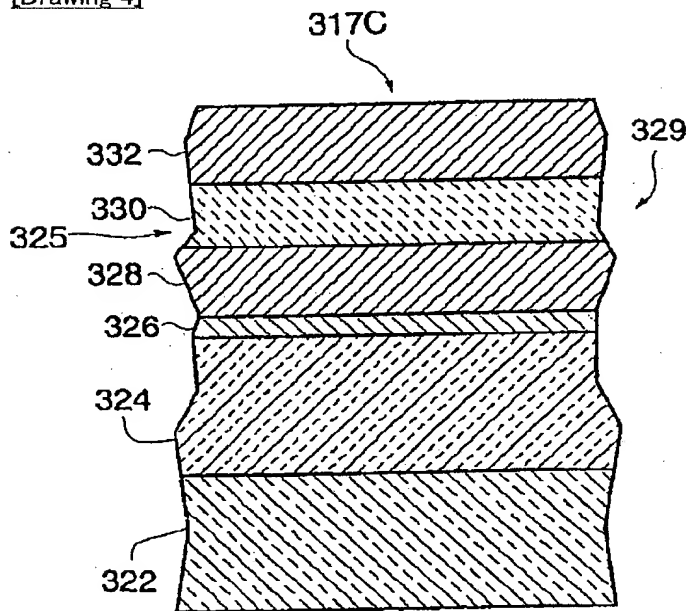


FIG. 2

[Drawing 3]

**FIG. 3**

[Drawing 4]

**FIG. 4**

[Drawing 5]

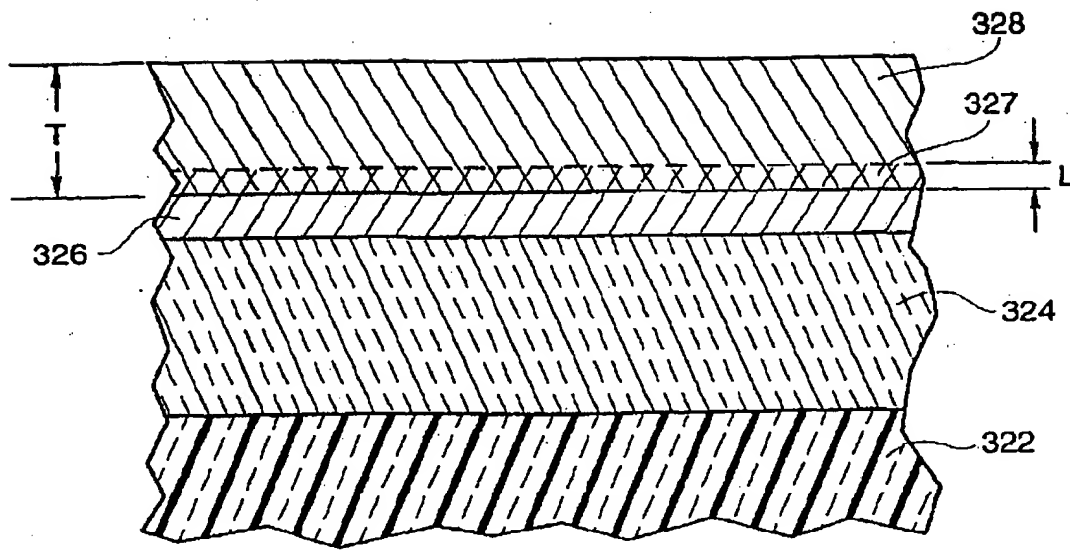


FIG. 5

[Translation done.]